ABSTRACT

An apparatus, method, and computer program for testing an integrated circuit comprising a plurality of clocked storage elements each having a clock input, wherein the clocked storage elements are interconnected by a plurality of signal paths, the apparatus comprising a control circuit adapted to provide a control signal; and a signal generator adapted to receive a first clock signal comprising k pulses each having a first duration, change the duration of each of m of the pulses to a second duration in response to the control signal, wherein $m < k$ and the second duration is not substantially equal to the first duration, to produce a second clock signal, and apply the second clock signal to the clock inputs of the plurality of clocked storage elements.